# CS 4141 — Digital Systems Laboratory, Lab 2 — Pre-Lab

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### How many select bits are used for the 4:1 Mux?

2 select bits - S1 and S0

### Which select bit is the most significant bit?

S1

### Suppose S1 = 1, S0 = 0 and 1G = 0, then which signal will be assigned to output 1Y?

D2

### Now we still have S1 = 1, S0 = 0 but 1G = 1, then what will 1Y be?

0/LOW

### Notice that we also have another set of inputs 2D and output 2Y. Explain how 2Y is related to 2D in one or two sentences.

2Y gives the value of the 2D corresponding to S0 and S1. In other words, it is another multiplexer with S0 and S1 and select bits, $2D_i$ as the data bits, and 2Y as the output.

### Given G1 and G2 are two enable pins. For the decoder to function, which logic value should we assign to G1 and G2?

Both G1 and G2 should be set to L, since otherwise the output of the decoder is all H, without regard to the input

### In a decoder, basically we select one output (among all outputs) based on the inputs. Suppose we set the enable pins correctly, and we set A = 0, B = 1, C = 0, D = 1, which output is chosen?

Output 10. This is since $1010_2 = 10_{10}$

### The chosen output is high or low based on the IC pinout?

The chosen output is low based on the IC pinout.

### Given that the output number indicates the decimal value of the inputs, which input (A or B or C or D) should be considered the most significant bit?

D should be considered the most significant bit.

### Given that the output number indicates the decimal value of the inputs, which input (A or B or C or D) should be least significant bit?

A should be the least significant bit.

## Implement the following Boolean function using 4:1 Multiplexer.

$$Y_1 = A'B'C' + A'BC + AB'C$$

## Make a truth table that describes the problem. Design a logic circuit that will output HIGH when the input is an odd number less than 8,and an even number greater than or equal to 8, and all inputs are smaller than 16. The input should be a 4-bit binary number. Design the circuit using a 4:16 decoder and other gates.

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |