CS 4141 — Digital Systems Laboratory, Lab 2 — Post-Lab

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$$F_1 = x'y + xy' + xz$$

x	y	z	F1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

$$F_2 = x'y'z + x'yz' + xy'z' + xyz$$

x	y	z	F2
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Full Adder Truth Table

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder Logic Diagram

Sum

Carry

* Note that the two diagrams may be combined into a single decoder chip by simply "overlapping" the two circuits.

Citations

Logic diagrams made using https://logic.ly/demo/